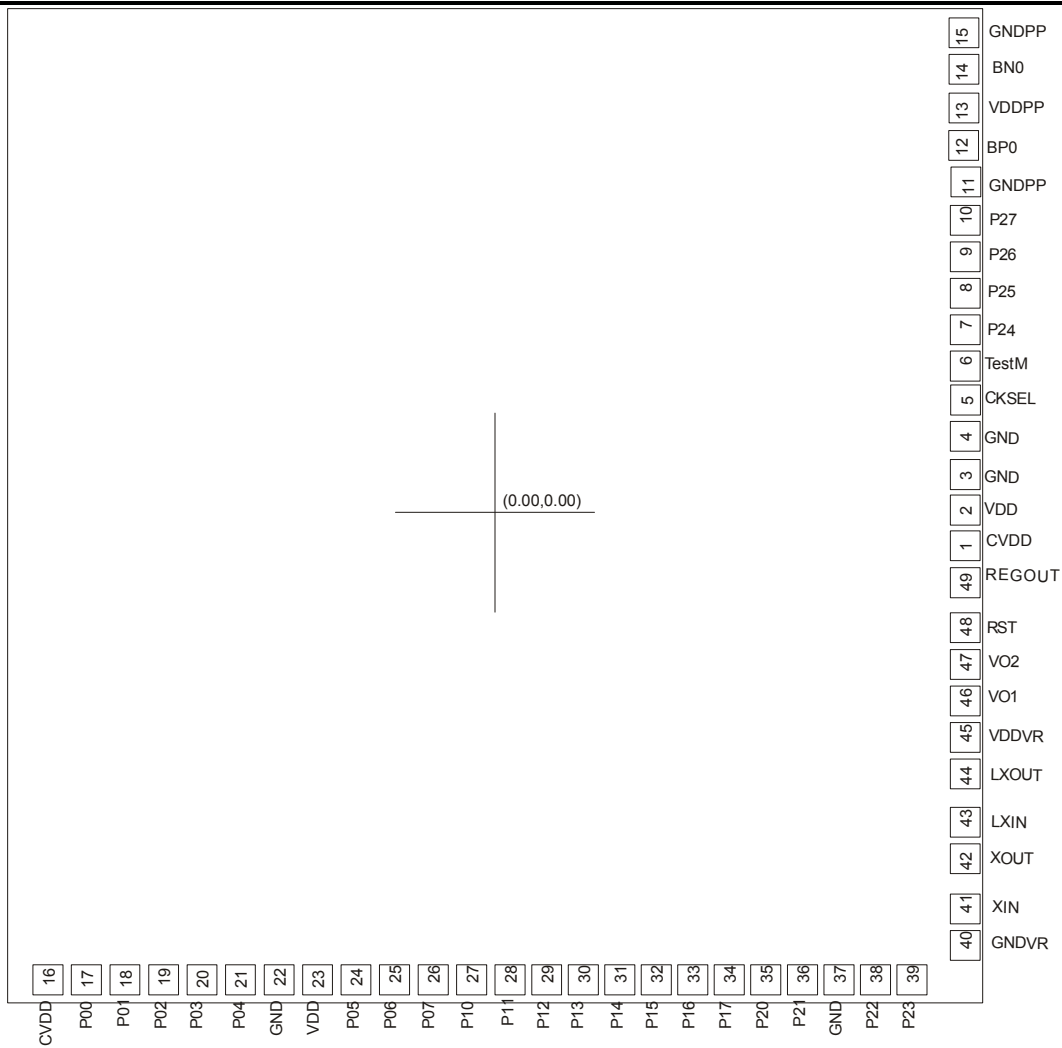


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**PROJECT: SNC88269A**

NO	PAD NAME	X(um)	Y(um)	NO	PAD NAME	X(um)	Y(um)
1	CVDD	1607.64	-188.24	25	P06	-596.19	-1597.00
2	VDD	1607.64	-52.09	26	P07	-486.19	-1597.00
3	GND	1607.64	57.91	27	P10	-376.19	-1597.00
4	GND	1607.64	167.91	28	P11	-266.19	-1597.00
5	CKSEL	1607.64	277.91	29	P12	-156.19	-1597.00
6	TestM	1607.64	387.91	30	P13	-46.19	-1597.00
7	P24	1607.64	497.91	31	P14	63.81	-1597.00
8	P25	1607.64	607.91	32	P15	173.81	-1597.00
9	P26	1607.64	717.91	33	P16	283.81	-1597.00
10	P27	1607.64	827.91	34	P17	393.81	-1597.00
11	GNDPP	1574.64	1022.47	35	P20	503.81	-1597.00
12	BP0	1574.64	1132.47	36	P21	613.81	-1597.00
13	VDDPP	1574.64	1293.16	37	GND	723.81	-1597.00
14	BN0	1574.64	1453.86	38	P22	833.81	-1597.00
15	GNDPP	1574.64	1563.86	39	P23	943.81	-1597.00
16	CVDD	-1586.19	-1597.00	40	GNDVR	1607.64	-1546.51
17	P00	-1476.19	-1597.00	41	XIN	1607.64	-1436.51
18	P01	-1366.19	-1597.00	42	XOUT	1607.64	-1284.91
19	P02	-1256.19	-1597.00	43	LXIN	1607.64	-1174.91
20	P03	-1146.19	-1597.00	44	LXOUT	1607.64	-1029.31
21	P04	-1036.19	-1597.00	45	VDDVR	1607.64	-919.31
22	GND	-926.19	-1597.00	46	VO1	1607.64	-809.31
23	VDD	-816.19	-1597.00	47	VO2	1607.64	-699.31
24	P05	-706.19	-1597.00	48	RST	1607.64	-533.61
				49	REGOUT	1607.64	-295.31



## SNC88269A

CHIP SIZE: X=3320um,Y=3298um

**Note: The substrate MUST be connected to GND in PCB layout**